I Claim:

1. A compensation component, comprising:

a semiconductor body having:

a surface;

two active zones;

a drift path disposed between said two active zones; and

a stacked layer sequence made up of regions of first and second conduction types, said regions having:

a lateral section with at least one end; and

at least one inclined section leading toward said surface of said semiconductor body and adjoining said end of said lateral section, said lateral section and said at least one inclined section being completely embedded in said semiconductor body.

2. The compensation component according to claim 1, wherein:

said lateral section has two ends; and

an inclined section is disposed at each of said two ends.

3. The compensation component according to claim 1, wherein said regions of said first conduction type are connected, at an end of said lateral section opposite said end adjoining said one inclined section, to a region of said first conduction type introduced at a low level as one of said two active zones.

4. The compensation component according to claim 3, wherein said region introduced at said low level is a drain zone.

5. The compensation component according to claim 1, wherein said stacked layer sequence is disposed in a mirror-image fashion with respect to at least one of said two active zones.

6. The compensation component according to claim 1, wherein at least one of said regions of said first conduction type is a proton irradiated region doped with at least one of the group consisting of a doping, phosphorus, and arsenic.

7. The compensation component according to claim 6, wherein at least one of said regions of said second conduction type is a boron-doped region.

8. The compensation component according to claim 1, wherein at least one of said regions of said second conduction type is a boron-doped region.

9. The compensation component according to claim 1, further comprising an SOI structure, said semiconductor body being disposed in said SOI structure.

10. The compensation component according to claim 1, wherein said semiconductor body is one of the group consisting of a MOSFET, a JFET, an IGBT, and a Schottky diode.

11. The compensation component according to claim 10, further comprising a terminal, said semiconductor body having at least two gate electrodes combined by a connection and commonly connected to said terminal.

12. The compensation component according to claim 1, wherein:

only regions of one of said first and second conduction types are introduced into a region of another of said first and second conduction types in said drift path; and

said other region is diffused to a low level.

13. The compensation component according to claim 1, wherein at least one of said regions of said first conduction type and said regions of said second conduction type of said lateral section and of said inclined section of said drift path are ion implanted with a mask having inclined edges.

14. The compensation component according to claim 1, wherein at least one of said regions of said first conduction type and said regions of said second conduction type of said lateral section and of said inclined section of said drift path are inclined-edged-masked ion implanted.

15. A method for fabricating the compensation component according to claim 1, which comprises:

providing a semiconductor body having:

a surface;

two active zones;

a drift path disposed between the two active zones; and

a stacked layer sequence made up of regions of first and second conduction types, the regions having:

a lateral section with at least one end; and

at least one inclined section leading toward the surface of the semiconductor body and adjoining the end of the lateral section, the lateral section and the at least one inclined section being completely embedded in the semiconductor body; and

fabricating at least one of regions of the first conduction type and regions of the second conduction type of the lateral section and of the inclined section of the drift path by ion implantation with a mask having inclined edges.

16. The method according to claim 15, which further comprises carrying out the ion implantation steps using different energy levels.

17. The method according to claim 15, which further comprises introducing the regions of the second conduction type by diffusion of a common region, which has diffused to a low level, into the semiconductor body.

18. The method according to claim 15, which further comprises fabricating the mask by:

applying an insulation layer is applied to the semiconductor body;

carrying out a damage implantation step in a surface region of the insulation layer;

applying a photoresist layer to the insulation layer, and exposing and developing the photoresist layer; and

wet etching the insulation layer masked by the photoresist layer.

19. The method according to claim 18, which further comprises applying a silicon dioxide insulation layer to the semiconductor body.

20. The method according to claim 18, which further comprises densifying the insulation layer before carrying out the damage implantation step.

21. The method according to claim 15, which further comprises introducing the active zones into the semiconductor body prior to the ion implantation step.

22. The method according to claim 15, which further comprises applying the mask to a protective layer located on the

semiconductor body to permit the mask to be removed without adversely affecting existing structures.

23. The method according to claim 22, which further comprises applying the protective layer on the semiconductor body as a silicon nitride protective layer.

24. The method according to claim 18, which further comprises applying the mask to a protective layer located on the semiconductor body to permit the mask to be removed without adversely affecting existing structures.